REMARKS

Claims 1-12 and 22-25 are currently pending. Claim 25 was rejected under 35 U.S.C. §102(e) and being anticipated by U.S. Patent 6,577,535 (Pasternak). Claims 1-12 and 22-24 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,005,812 (Mullarkey) in view of U.S. Patent No. 5,796,285 (Drouot) and U.S. Patent No. 6,249,473 (Lau).

Regarding the rejection of independent Claim 25 under §102(e) the Examiner states that Pasternak anticipates each and every limitation of the claim. Applicants respectfully disagree.

Claim 25 recites a DC voltage generator system for supplying at least one voltage level to a plurality of subsystems on an integrated circuit having a system on chip (SOC) design.

Pasternak teaches a method and system for distributed power generation in multi-chip memory systems. The system of Pasternak is applicable to multiple memory chips. For example memory blocks 304-310 are individual chips. These chips are shown on a memory board 500 in FIG. 5. A board is not a chip; a board has a controller and many chips. This board design is what is known in the prior art.

The present invention relates to multiple and various systems that are integrated on a single chip, i.e. a system on chip (SOC) design. A board is not and cannot be equated with an SOC design.

It is well known that the technical requirements to design an SOC are extensive. The process requires extensive cross-field skills, experience and tools in order to design a properly functioning SOC.

Applicants respectfully submit the following table to support the position that a board is not and cannot be equated with an SOC.

Item	Chips on a board	System on Chip (SOC)
Power supply	Easy to supply power; each chip is individually controlled	Difficult to supply power since sub-systems are interconnected when power is switched off from a chip; individual sub-systems cannot be supplied power easily
Controls	Easy to control each chip; each chip is more or less operated independently	Control is a complex process; one control can affect the other, or the chip will be too bulky to be practical
Power management	Simple, if any chip is not in use, the chip can be switched off, and vice versa.	More difficult, due to sharing hardware among sub-systems, one cannot arbitrarily switch on or off a subsystem; a sophisticated design is necessary to squeeze the chip size and manage the power; this involves the claimed DC design
Layout arrangement	Simple; can place as many chips as space on the board will allow; placement of the chips where clock can be distributed evenly; little noise concern	Difficult challenge; signal flow, power line distribution, power dissipation, clock distribution, cross-talk noise, sharing components, etc...
Performance	Fixed, old design	Sufficient room to improve, since the distance between systems are much closer than before.

Accordingly, for at least the above-stated reasons, it is respectfully requested that the rejection of Claim 25 under 35 U.S.C. §102(e) be withdrawn.

Regarding the rejection of independent Claims 1 and 23 under 35 U.S.C. §103(a), the Examiner states that the combination of Mullarkey in view of Drouot and Lau teach each and every limitation of the claim. Applicants respectfully disagree.

Again, each of Claims 1 and 23 recite a DC voltage generator system for supplying at least one voltage level to a plurality of subsystems on an integrated circuit having a system on chip (SOC) design.

Initially, since each of Mullarkey, Drouot and Lau teach systems of individual chips, and not a SOC design, the arguments recited above with respect to Claim 25 are applicable to Claims 1 and 23.

Claims 1 and 23 recite a plurality of local DC voltage generators distributed throughout the SOC chip, each local DC voltage generator independently supplying voltage to at least one unit of the plurality of subsystems. Drouot does not teach or disclose to a plurality of local DC voltage generators distributed throughout the SOC design, as recited by Claims 1 and 23.

Moreover, the SOC design, as defined by Claims 1 and 23, includes a plurality of subsystems having a plurality of units. The Examiner equates the plurality of subsystems having a plurality of units with elements (84), (86), (88), and (90) of Mullarkey. However, with reference to Column 5, Lines 5-11, Mullarkey, teaches an electronic system (82) includes an input device (84), an output device (86), a processor device (88), and a memory device (90) which are shown as separate units in FIG. 3 of Mullarkey. Mullarkey then teaches the any of one of the input, output, and processor devices can also incorporate the DRAM device (10). In other words, according to DRAM device (10) can be incorporated with an input, output or processor devices. However, this does not teach or suggest the recitation of a plurality of local DC voltage generators distributed throughout the SOC design, each local DC voltage generator independently supplying voltage to at least one unit of the plurality of subsystems, as recited by Claims 1 and 23.

The features of Claims 1 and 23 are neither taught nor disclosed by any combination of Mullarkey, Drouot and Lau.

Accordingly, for at least the above-stated reasons, it is respectfully requested that the rejection of Claims 1 and 23 under 35 U.S.C. §103(a) be withdrawn.

Independent Claims 1, 23 and 25 are believed to be in condition for allowance. Without conceding the patentability per se of dependent Claims 2-12, 22, and 24, these are likewise believed to be allowable by virtue of their dependence on their respective amended independent claims. Accordingly, reconsideration and withdrawal of the rejections of dependent Claims 2-12, 22, and 24 is respectfully requested.

Accordingly, all of the claims pending in the Application, namely, Claims 1-12 and 22-25, are believed to be in condition for allowance. Should the Examiner believe that a telephone conference or personal interview would facilitate resolution of any remaining matters, the Examiner may contact Applicants' attorney at the number given below.

Respectfully submitted,

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